InAlAs/InGaAs/InP-HEMT TECHNOLOGIES FOR HIGH-YIELD ANALOG/DIGITAL ICS

Yohtaro Umeda, Takatomo Enoki, Kazuo Osafune, Hiroshi Ito, and Yasunobu Ishii

NTT LSI Laboratories
3-1 Morinosato Wakamiya, Atsugi-shi
Kanagawa, 243-01 Japan

ABSTRACT

High-yield and high-performance digital/analog ICs have been fabricated using the same InAlAs/InGaAs/InP-HEMT process. SCFL static frequency dividers show a fabrication yield of 63% and operate at 36.7 ±0.55 GHz. Two-stage MMIC-LNAs show a yield of 75% and at 62 GHz a noise figure of 4.3 ±0.19 dB and a gain of 11.8 ±0.25 dB.

INTRODUCTION

InAlAs/InGaAs/InP HEMTs have demonstrated ultra-high-speed and low-noise performance and have been applied to various MMICs for the mm-wave band. We have already reported monolithic low-noise amplifiers (MMIC-LNA) for 26-, 40-, and 50-GHz bands on MBE wafers [1], [2], [3] and have also developed the first successful InAlAs/InGaAs/InP-HEMT process for digital ICs by introducing an InP recess-etch stopper [4], [5] grown by MOCVD. This process enabled us to make a source-coupled-FET-logic (SCFL) static frequency divider operating at 40.4 GHz [5]. The next step is to integrate analog and digital circuits into one chip. This will make it possible to build, for instance, one-chip phase-locked-loop ICs for frequency synthesizers or monolithic front-end ICs including a preamplifier and decision circuit for optical transmission systems. In addition, the monolithic integration of such circuits can reduce the degradation of the circuit performance and lower the cost of circuit modules during the implementation to fixtures. Moreover, in millimeter-wave region, interfaces between these discrete circuits becomes extremely difficult as the frequency increases. Therefore, this integration is considered to be essential for the future ultra-high-speed radio- and optical-transmission systems. This integration, however, requires that both the analog and digital ICs be fabricated using the same IC process. It is also necessary to improve yield and uniformity while maintaining the performance of both kinds of ICs.

This paper reports a study on the feasibility of monolithically integrating analog and digital circuits by using the InAlAs/InGaAs/InP HEMT process. An MMIC-LNA was used as the analog test circuit so that we could evaluate the fundamental performance of analog ICs (i.e., their gain and noise characteristics). An SCFL frequency divider was used as the digital test circuit because this kind of circuit reveals the basic operations of SCFL gates. The applicability of the HEMT process to both ICs is examined separately here by presenting the yield and uniformity, as well as the performance, for both ICs.

InAlAs/InGaAs/InP HEMT TECHNOLOGIES

InAlAs/InGaAs modulation-doped heterostructure lattice-matched to InP substrate was grown by MOCVD. Figure 1 shows a cross section of a HEMT with a gate length of 0.1 μm. Although mushroom-shaped gates formed with a multilayer resist system are commonly used, their production requires critical control of EB exposure and development. Therefore, to increase productivity, direct EB delineation was used to form a T-shaped-gate for the gate footprint and optical lithography was used to form the top part of the gate electrode [6]. To ensure uniformity of gate-recess depth, an InP layer was inserted into the InAlAs barrier layer as a gate-recess-etch stopper. The InP etch stopper is compatible with the n^+-InGaAs/n^+-InAlAs cap layer used for non-alloyed ohmic contact [6] in the fabrication process. The interconnection lines were composed of one-layer metal with air-bridge crossovers, which was developed for

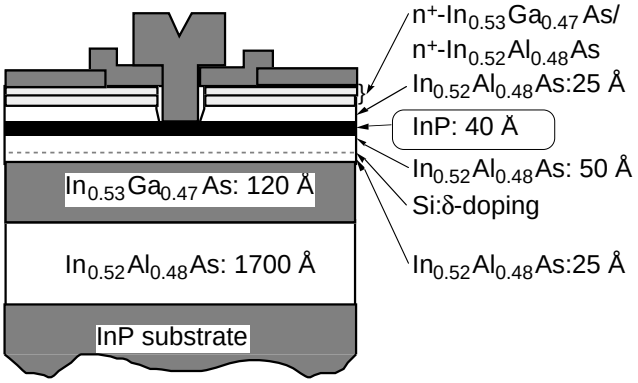

Fig. 1. Structure of an InAlAs/InGaAs/InP HEMT with an InP recess-etch stopper.

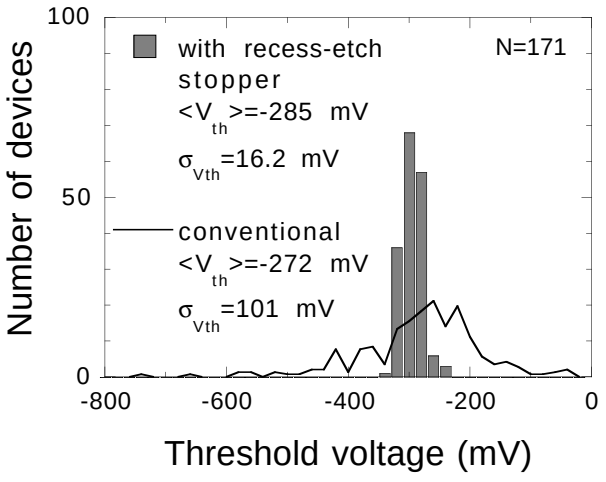

Fig. 2. Threshold voltage (V_{th}) distribution on a two-inch wafer of 0.1-μm-gate MOCVD-based HEMTs with an InP-recess-etch stopper and of MBE-based ones without an recess-etch stopper.

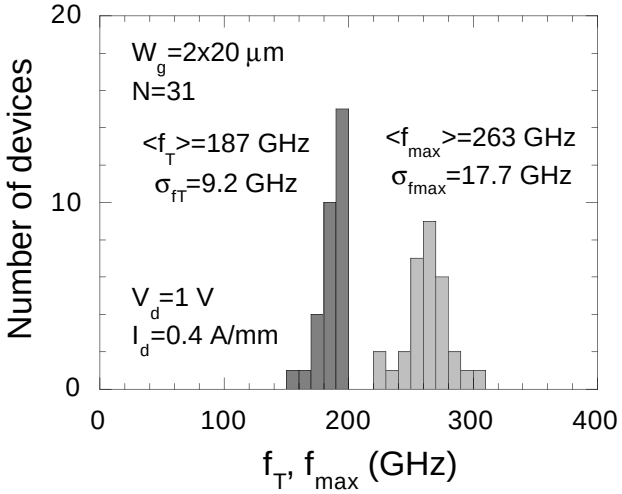

Fig. 3. Distribution on a two-inch wafer of current-gain cuttoff frequency (f_T) and maximum oscillation frequency (f_{max}) of the 0.1-μm-gate MOCVD-based HEMTs with an InP-recess-etch stopper.

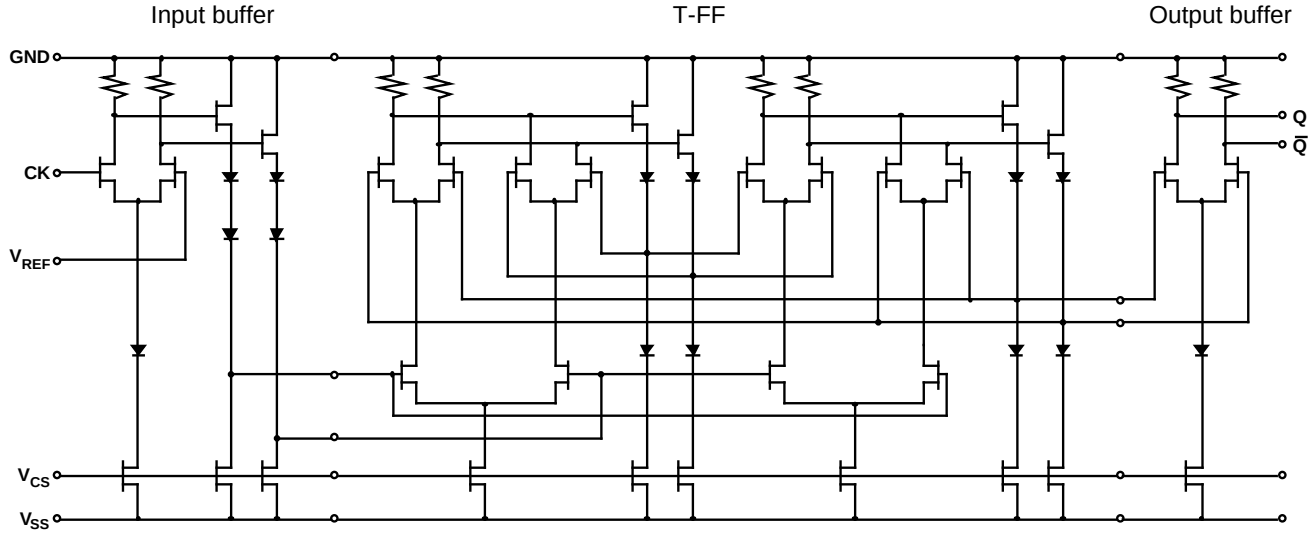

Fig. 4. Circuit diagram of an SCFL static frequency divider.

the conventional MMIC process. Figure 2 shows the threshold voltage (V_{th}) distribution for the HEMTs on a two-inch wafer. For comparison, the distribution for conventional HEMTs without a recess-etch stopper is also shown. When using the conventional process to make HEMTs, it is difficult to reduce the V_{th} standard deviation (σ) to less than 100 mV. By using InP recess-etch stopper, however, it was possible to reduce σ to only 16 mV. The average transconductance was as high as 1.34 S/mm with a σ of 75 mS/mm. Figure 3 shows the distribution of current-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) estimated from measured S-parameters by -6 dB/octave extrapolation of current gain and Mason's unilateral power gain, respectively. 31 of 32 samples of the HEMTs on a two-inch wafer worked well and showed a very high average f_T and f_{max} of 187 and 263 GHz with a small σ of 9.2 and 17.7 GHz, respectively. These results shows excellent yield and uniformity of the rf and dc characteristics of the HEMTs. These performance values are considered to be sufficient for application to high-yield small-scale integration for analog/digital ICs.

FREQUENCY DIVIDER

SCFL static binary frequency dividers were fabricated in order to examine the applicability of the HEMT-IC process to digital ICs. The circuit diagram and a micrograph of a

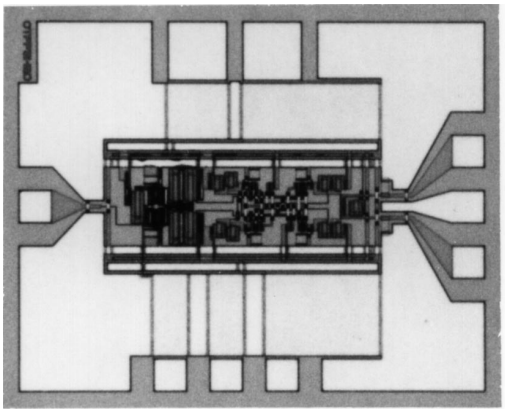

Fig. 5. Photomicrograph of a frequency divider.

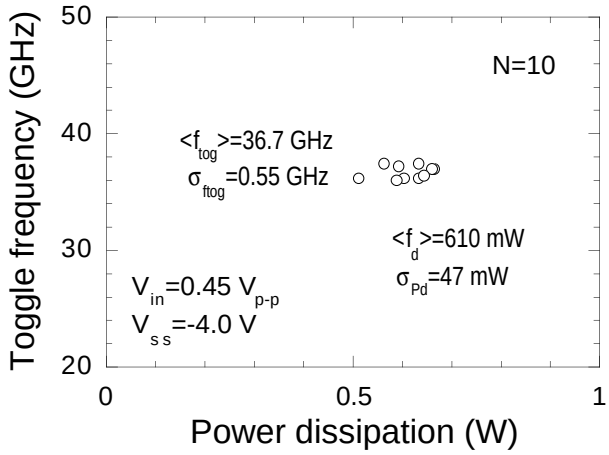

Fig. 6. Distribution of toggle frequency (f_{tog}) and power dissipation (P_d) of frequency dividers.

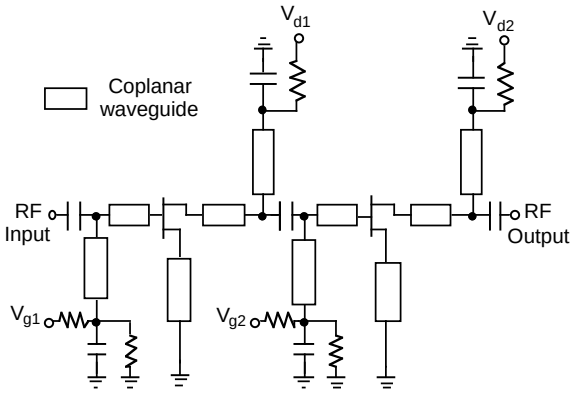

Fig. 7. Circuit diagram of two-stage MMIC-LNA.

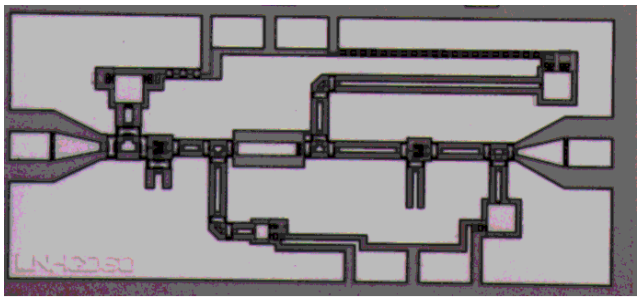

Fig. 8. Photomicrograph of a 60-GHz-band MMIC-LNA.

frequency divider are shown in Fig. 4 and 5. @The frequency divider includes an input buffer that transfers single-ended to differential form of signal, a toggle flip-flop (T-FF) using two D-latches, and an output buffer driving 50-Ω lines. It also uses 32 FETs, 14 Schottky diodes, 8 resistors using an active layer, and 5 metal-insulator-metal (MIM) capacitors. @The chip size was 1.25 x 1.0 mm, and the gate widths of the FETs for the input buffer, T-FF, and output buffer were respectively 50, 20, and 20 μm. The reason for the choice of 20-μm-wide-gate FETs for the T-FF is that this width minimizes the sum of the charging delay and the delay due to the interconnection lines and thus results in the fastest operation of the circuit [7]. The performance of the fabricated frequency dividers is shown in Fig. 6. Although the interconnection-line process is not yet optimized for digital ICs and consequently the delays due to the interconnections are still large [7], the average maximum toggle frequency on a two-inch wafer reached 36.7 GHz, with a σ of only 0.55 GHz. The average power dissipation was 610 mW with a σ of 47 mW. The yield for 16 samples in a 2- inch wafer is 63%. From this result, the yield for an FET was calculated to be 98.6%, assuming that the yield of the frequency divider depends only on FETs and the yields of FETs are independent of each other. This results agrees well with the high yield of the descrete HEMTs described in the previous section.

MMIC-LNA

60-GHz-band two-stage MMIC-LNAs were fabricated using the same fabrication process used to make the frequency dividers. Figures 7 and 8 show a circuit diagram and a photograph of the LNA. The chip consisted of two 25-μm-wide-gate HEMTs with two gate fingers, I/O matching stubs for each stage using coplanar waveguides, and biasing circuits using MIM capacitors and resistors. The chip size was 1.8 x 0.8 mm. The design is based on the uniplanar circuit configuration [8], which enables circuits to be fabricated on one side of a substrate. This configuration is advantageous in the monolithic integration of microwave and digital circuits on one chip because the fabrication process of uniplanar MMICs is compatible with that of the digital ICs. Stabilization results from the combination of transmission lines between the source of FETs and the ground

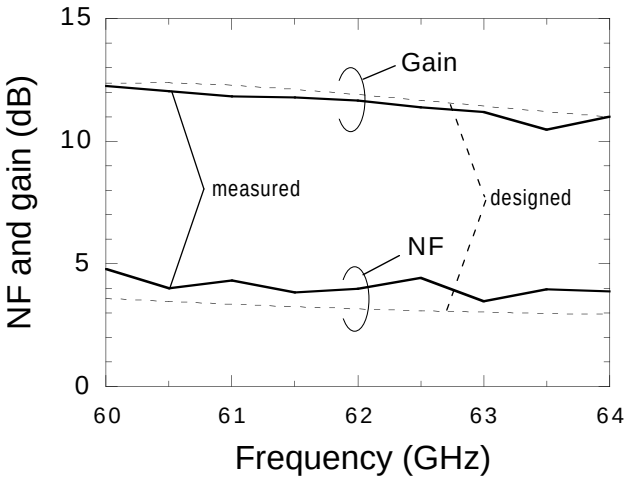

Fig. 9. Designed and measured frequency dependency of NF and gain for an MMIC-LNA.

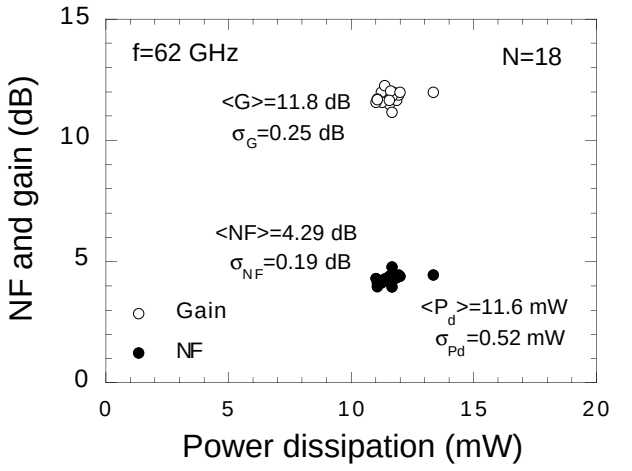

Fig. 10. Distribution of NF, gain (G), and power dissipation (P_d) for MMIC-LNAs on a two-inch wafer.

as negative feedbacks and from the parallel connections of a resistor and capacitor at the end of matching stubs as frequency-dependent power-loss elements. The former stabilize the amplifier in the use band without degradation of noise figure (NF), while the latter stabilize in the lower band of the use band. This stabilization method can minimize NF in the design with a compromise between NF and gain (G) [9]. Figure 9 shows that the designed and measured NF and G of the LNA agree well. Between 60 and 64 GHz the LNA showed an low average NF of 4.1 dB and a high average gain of 11.5 dB. Figure 10 shows the distribution of NF and G of the LNAs fabricated on a two-inch wafer. At 62 GHz the average NF and G were 4.3 and 11.8 dB with an extremely small σ of 0.19 and 0.25 dB, respectively. The yield for 24 samples on a two-inch wafer is 75 %. This high uniformity is also due to the uniformity of the HEMTs.

CONCLUSION

The applicability of the 0.1-μm-gate HEMT process to analog/digital ICs has been examined. The HEMT employing a T-shaped-gate and InP recess-etch stopper showed superior uniformity. Fabricated SCFL frequency dividers and MMIC-LNAs showed excellent yield, uniformity and performance. These results show that the small-scale monolithic integration of both analog and digital circuits onto one chip by using this HEMT process is both feasible and promising.

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